

IN THE CLAIMS:

Please enter the following claim set:

1-5. (canceled)

6. (previously presented) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:
a semiconductor substrate of a first conductivity type having a memory region;
a first well of a second conductivity type located in the memory region; and
a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;
wherein the non-volatile memory transistor is operated using voltages including positive and negative voltages;

wherein, for writing data in the non-volatile memory transistor, a voltage in an opposite polarity is applied to the control gate, a voltage in one polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for erasing data in the non-volatile memory transistor, a voltage in the one polarity is applied to the control gate, a voltage in the opposite polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for writing data in the non-volatile memory transistor, a voltage of -3 V through -4 V is applied to the control gate, a voltage of +3 V through +4 V is applied to one of the source and the drain, a voltage of -5 V through -6 V is applied to the other of the source and the drain, a voltage of -5 V through -6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well; and

wherein, for erasing data in the non-volatile memory transistor, a voltage of +6 V through

+7 V is applied to the control gate, a voltage of -5 V through -6 V is applied to one of the source and the drain, a voltage of -5 V through -6 V is applied to the other of the source and the drain, a voltage of -5 V through -6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well.

7-14. (canceled)

15. (currently amended) A semiconductor device having a non-volatile memory transistor ~~according to claim 14, having a split-gate structure, the semiconductor device comprising:~~

a semiconductor substrate of a first conductivity type having a memory region;
a first well of a second conductivity type located in the memory region;
a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;
wherein the non-volatile memory transistor has a gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the gate insulation layer is located above the second well and between one of the source and drain and the other of the source and drain,
the floating gate is located above the first gate insulation layer,
the intermediate insulation layer is located above the floating gate and the semiconductor substrate, and
the control gate is located above the intermediate insulation layer and rests on the floating gate through the intermediate insulation layer;
wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein
the first transistor region includes a first voltage-type transistor that operates at a first voltage level,
the second transistor region includes a second voltage-type transistor that operates at a second voltage level, and
the third transistor region includes a third voltage-type transistor that operates at a third

voltage level,

wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed;

wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

wherein the intermediate insulation layer of the non-volatile memory transistor is formed from at least three insulation layers, wherein first and second outermost layers of the three insulation layers respectively contact the floating gate and the control gate and are formed from a thermal oxidation method;

wherein the intermediate insulation layer includes an insulation layer between the first and the second outermost layers, that is formed by a CVD method; and

wherein the insulation layer between the first and second outermost layers that is formed by a CVD method is a silicon oxide layer formed by a CVD method selected from a group consisting of a HTO (high temperature oxide) method and a TEOS (tetraethyl orthosilicate) method.

16-21. (canceled)

22. (currently amended) A semiconductor device having a non-volatile memory transistor according to claim 14, having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region;

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor has a gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the gate insulation layer is located above the second well and between one of the source

and drain and the other of the source and drain,

the floating gate is located above the first gate insulation layer,

the intermediate insulation layer is located above the floating gate and the semiconductor substrate, and

the control gate is located above the intermediate insulation layer and rests on the floating gate through the intermediate insulation layer;

wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein

the first transistor region includes a first voltage-type transistor that operates at a first voltage level,

the second transistor region includes a second voltage-type transistor that operates at a second voltage level, and

the third transistor region includes a third voltage-type transistor that operates at a third voltage level,

wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed;

wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

wherein the intermediate insulation layer of the non-volatile memory transistor is formed from at least three insulation layers, wherein first and second outermost layers of the three insulation layers respectively contact the floating gate and the control gate and are formed from a thermal oxidation method;

wherein the intermediate insulation layer includes an insulation layer between the first and the second outermost layers, that is formed by a CVD method; and

wherein the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor has a film thickness of 5 – 15 nm, and the second outermost layer has a film thickness of 1 – 10 nm, and the layer formed between the first and the second outermost layers comprises a silicon oxide layer having a film thickness of 10 – 20 nm.

23. (canceled)

24. (previously presented) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

- a semiconductor substrate of a first conductivity type having a memory region;
- a first well of a second conductivity type located in the memory region;
- a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;
- wherein the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer;
- wherein the first gate insulation layer and the second gate insulation layer are located above the second well and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer;
- wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein the first transistor region includes a first voltage-type transistor that operates at a first voltage level of 1.8 - 3.3 V, the second transistor region includes a second voltage-type transistor that operates at a second voltage level of 2.5 - 5 V, and the third transistor region includes a third voltage-type transistor that operates at a third voltage level of 10 - 15 V; and
- wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

25. (canceled)

26. (currently amended) A semiconductor device having a non-volatile memory transistor according to claim 25, having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;
a first well of a second conductivity type located in the memory region;
a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;
wherein the non-volatile memory transistor has a gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the gate insulation layer is located above the second well and between one of the source and drain and the other of the source and drain,
the floating gate is located above the first gate insulation layer,
the intermediate insulation layer is located above the floating gate and the semiconductor substrate, and
the control gate is located above the intermediate insulation layer and rests on the floating gate through the intermediate insulation layer;
wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein
the first transistor region includes a first voltage-type transistor that operates at a first voltage level,
the second transistor region includes a second voltage-type transistor that operates at a second voltage level, and
the third transistor region includes a third voltage-type transistor that operates at a third voltage level,
wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed;
wherein the semiconductor device further comprises at least a flash-memory (flash EEPROM), wherein the flash-memory includes a memory cell array comprising non-volatile memory transistors and peripheral circuits formed therein; and

wherein the semiconductor device further comprising comprises another circuit region mixed together with the flash-memory (flash EEPROM) on the substrate.

27. (previously presented) A semiconductor device having a non-volatile memory transistor according to claim 26, wherein the circuit region includes at least a logic circuit.

28-32. (canceled)

33. (currently amended) A semiconductor device ~~according to claim 1, wherein~~ having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;
a first well of a second conductivity type located in the memory region; and
a second well of a first conductivity type located in the first well, wherein the non-volatile
memory transistor includes a source and drain that are located in the second well;

wherein the semiconductor substrate further includes first, second and third transistor regions including first, second and third field effect transistors that operate at different voltage levels, the second field effect transistor including a gate insulation layer formed from two silicon oxide layers, and the third field effect transistor including a gate insulation layer formed from three silicon oxide layers.

34. (currently amended) A semiconductor device ~~according to claim 31, having a~~ non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;
a first well of a second conductivity type located in the memory region;
a second well of a first conductivity type located in the first well, wherein the non-volatile
memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor having a split gate structure comprises a
source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to

act as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is composed of at least three insulation layers, wherein a first layer of the three insulation layers contacts the floating gate, a third layer contacts the control gate, and a second layer is located between the first and third layers; and

wherein the second layer of the intermediate insulation layer is silicon oxide.

35. (previously presented) A semiconductor device according to claim 33, wherein the non-volatile memory transistor includes a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to act as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer includes at least three insulation layers, wherein a first layer of the at least three insulation layers contacts the floating gate, a third layer of the at least three insulation layers contacts the control gate, and a second layer of the at least three insulation layers is located between the first and third layers, wherein the first, second, and third layers each comprise silicon oxide.